

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Japanese Patent Application No.

- 5 11-369811, filed December 27, 1999, the entire subject matter of which is incorporated  
herein of reference.

BACKGROUND OF THE INVENTION

1. Field of the invention

10 The invention relates to a semiconductor device, which has at least one dummy  
pattern to protect wiring patterns from corrosion.

2. Description of the related art

A semiconductor device having metalized wiring pattern in the related art is  
15 formed in the process described below with reference to Figs. 8A through 8C.

Referring to Fig. 8A, a semiconductor substrate 101 having circuit elements,  
such as transistors, in a circuit area of a chip area on its surface is prepared, and then,  
a metal layer which is formed of Aluminum are formed on the entire main-surface of  
the semiconductor substrate 101. Then, metalized wiring patterns 102 are formed by  
20 etching the metal layer to make an interconnection of the circuit elements.

Next, referring to Fig. 8B, a first insulating layer 103, such as a silicon oxide  
layer, is formed on the entire main-surface of the semiconductor substrate 101 and on

the exposed surface of the metalized wiring patterns 102 by the CVD process. After that, a SOG (Spin On Glass) layer 104 as a second insulating layer is coated on the first insulating layer 103 to planarized its surface. According to the spin coating process, the thick SOG layer is formed in an area where no wiring patterns is formed, 5 and the thin SOG layer is formed on the wiring patterns. Then, a third insulating layer 105, such as a silicon oxide layer, is formed on the SOG layer by the CVD process.

After that, referring to Fig. 8C, the first insulating layer 103, the SOG layer 104, the third insulating 105 layer only in an grid line area is removed to make an opening 106 until the surface of the semiconductor is exposed. This process is very important 10 to avoid cracking the semiconductor device at the scribing process.

However, as the SOG layer is exposed at an edge 1000 of the opening 106, moisture comes into the semiconductor device because the SOG layer has hygroscopicity. As a result, the metalized wiring patterns are corroded.

## 15 SUMMARY OF THE INVENTION

An objective of the invention is to resolve the above-described problem and to provide a semiconductor device having a dummy pattern to protect wiring patterns formed in the semiconductor device from corrosion.

The objective is achieved by a semiconductor device including a semiconductor 20 substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area, circuit patterns formed on the substrate in the circuit area, a first dummy pattern which is formed of the same

material as the circuit pattern, formed in the dummy area, the dummy pattern encompassing the circuit area, a first insulating layer formed on an entire surface of the semiconductor substrate, a second insulating layer formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns; and a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

The objective is further achieved by a method for manufacturing a semiconductor device including a step for preparing a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area, a step for forming a conductivity layer on the semiconductor substrate, a step for forming circuit patterns in the circuit area and a dummy pattern encompassing the circuit area in the dummy area by etching the conductivity layer, a step for forming a first insulating layer formed on an entire surface of the semiconductor substrate, a step for forming a second insulating layer on the first insulating layer, a step for removing the second insulating layer which is formed on the first insulating layer on the dummy pattern until the surface of the first insulating layer is exposed, a step for forming a third insulating layer formed on the exposed first insulating layer and on the second insulating layer; and , a step for removing the first, second and third insulating layers in the grid-line area.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more particularly described with reference to the accompanying drawings in which:

- Figs. 1A through 1C are sequential sectional views for forming a semiconductor device of a first of fifth illustrative embodiments of the invention;

Fig. 2A is a graph showing a relationship between the thickness of a SOG layer formed on the dummy pattern and the width ( $L_w$ ) of the dummy pattern or the length ( $L_s$ ) between the dummy pattern and metalized wiring pattern, of the first embodiment;

- Fig. 2B is an enlarged sectional view at the edge of the circuit area to indicate the width ( $L_w$ ) and the length ( $L_{s1}$ ) which is used in Fig. 2A;

Figs. 3A through 3C are sequential sectional views for forming a semiconductor device of a second of fifth illustrative embodiments of the invention;

- Fig. 4A is a graph showing a relationship between the thickness of a SOG layer formed on the second dummy pattern and the width ( $L_w$ ) of the second dummy pattern or the length ( $L_{s1}$ ) between the second dummy pattern and metalized wiring pattern, of the second embodiment;

Fig. 4B is an enlarged sectional view at the edge of the circuit area to indicate the width ( $L_w$ ) and the length ( $L_{s1}$ ) which is used in Fig. 4A

- Figs. 5A through 5E are sequential sectional views for forming a semiconductor device of a third of fifth illustrative embodiments of the invention;

Fig. 6 is a sectional view of a semiconductor device of a fourth of fifth illustrative

embodiments of the invention;

Fig. 7a is a sectional view of a semiconductor device of a fifth of fifth illustrative embodiments of the invention;

Fig. 7b is an enlarged plan view of the semiconductor device shown in Fig. 7a;

5 and

Figs. 8A through 8C are sequential sectional views for forming a semiconductor device in the related art.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

10 Referring to Fig. 1A, unillustrated circuit elements, such as transistors, are formed in a circuit area of the chip area on a main-surface of the semiconductor substrate 201, and then, an unillustrated insulating layer is formed on the surface of the semiconductor substrate 201. Next, a metal layer having a thickness of 600nm, which is formed of Aluminum, is formed on the entire main-surface of the  
15 semiconductor substrate 201, and then, metalized wiring patterns 202 are formed in the circuit area by etching the metal layer to make an interconnection of the circuit elements. Simultaneously, a dummy pattern 202a, which is electrically isolated from the wiring pattern 202, is formed in a dummy area by etching the metal layer. The dummy area is disposed between the circuit area and the grid-line area. A  
20 manufacturing margin area is located on either side of the dummy area from the circuit area and grid-line area, respectively. For example, a frame-shaped dummy area having a width of  $((1000-0.05)-(800+0.05))/2 \mu\text{m}$  is formed, providing that the chip

area has  $1000 \times 1000 \mu\text{m}$ , the circuit area whose center is correspondence to a center of the chip area, has  $800 \times 800 \mu\text{m}$ , and width of the manufacturing margin is  $0.05 \mu\text{m}$ . Therefore, the circuit area is encompassed with the dummy area. Although the dummy pattern 202a can be formed in the dummy area, preferably, the distance (L) 5 between the edge 1000 of the chip area and an outer edge of the dummy pattern 202a is set for over  $10 \mu\text{m}$ .

Next, referring to Fig. 1B, a first insulating layer 203, such as silicon oxide layer, having a thickness of 200nm is formed by CVD on the entire surface of the semiconductor substrate 201. Then, a SOG layer 204 as a second insulating layer is 10 ~~coated only on~~ 10 the first insulating layer 203 which is directly formed on the semiconductor substrate 201 and which is formed on the metalized wiring patterns 202 to planarize the surface. That is, the SOG layer is not formed on the first insulating layer 203, which is formed on the dummy pattern 202a. The condition not to be formed the SOG layer on the dummy pattern is explained later. Then, a third 15 insulating layer 205 having a thickness of 400nm is formed by CVD on the SOG layer 204 and the exposed first insulating layer 203 which is formed on the dummy pattern 202a.

Then, referring to Fig. 1C, the first insulating layer 203, the SOG layer 204, and the third insulating layer 205 on the grid line area are removed until the surface of the 20 semiconductor substrate 201 is exposed.

In the process shown in Fig. 1B, the SOG layer is coated in the following condition and the thickness of the SOG layer 204 on the dummy pattern 202a is

measured in changing the width ( $L_w$ ) of the dummy pattern 202a or the length (Ls1) between the dummy pattern 202a and metalized wiring pattern 202. A result of the measurement is shown in Fig. 2A.

- (1) the material of the SOG layer: Concentration of Solid content is 5.2wt%
- 5 (2) the material of the SOG layer: Viscosity is 1.03 mPa.sec.
- (3) Rotary speed: 5000 rpm

Referring to Figs. 2A and 2B, the X axis shows the thickness of the SOG layer on the dummy pattern 202a, and Y axis shows the width ( $L_w$ ) of the dummy pattern 202a or length (Ls1) between the dummy pattern 202a and metalized wiring pattern 10 202.

In Fig. 2A, the black circles shows the relationship between the thickness of the SOG layer and the width ( $L_w$ ) of the dummy pattern 202a where the length (Ls1) is fixed to  $2.6 \mu\text{m}$  and the width ( $L_w$ ) is changed from 1 to  $100 \mu\text{m}$ . In this case, it is found that if the width ( $L_w$ ) is getting wider, the SOG layer becomes thicker. The with 15 circles shows the relationship between the thickness of the SOG layer and the length (Ls1) where the width ( $L_w$ ) is fixed to  $1.0 \mu\text{m}$  and the length (Ls1) is changed from 0.9 to  $5 \mu\text{m}$ . In this case, it is found that the thickness of the SOG layer on the dummy pattern 202a is maintained to nearly zero even if the length (Ls1) is set until  $5 \mu\text{m}$ .

As a result form this experimentation, if the width ( $L_w$ ) is designed to  $1.0 \mu\text{m}$ , 20 the SOG layer is not formed on the dummy pattern 202a. Therefore, if the dummy pattern 202a having a width of  $1.0 \mu\text{m}$  is formed, the SOG layer 204 which is adjacent

to the grid-line area is completely isolated from the SOG layer 204 which is formed in the circuit area by the first insulating layer 203 formed on the dummy pattern 203.

According to the first embodiment of the invention, as the SOG layer 204 which is adjacent to the grid-line area is completely isolated from the SOG layer 204 which is 5 formed in the circuit area by the first insulating layer 203 formed on the dummy pattern 203, it is possible to protect the semiconductor device from moisture which comes into the semiconductor device through the SOG layer 204. Further, as the dummy pattern 202a can be formed with the metalized wiring patterns, simultaneously, it is not necessary to add some additional process. Furthermore, since the dummy pattern is 10 formed outside of the circuit area, the surface of the semiconductor device at the peripheral area is planarized as the additional effect of the dummy pattern.

The second embodiment is described below with reference to Figs. 3A through 3C and Figs. 4A through 4B. Referring to Fig. 3A, unillustrated circuit elements, such as transistors, are formed in a circuit area of the chip area on a main-surface of the 15 semiconductor substrate 201, and then, an unillustrated insulating layer is formed on the surface of the semiconductor substrate 201. Next, a tungsten polycide layer having a thickness of about 3000  $\mu\text{m}$  is formed on the insulating layer, and then, a lower dummy pattern 300a (a second dummy pattern) is formed in a dummy area by etching the tungsten polycide layer. As well as the dummy area decried in the first 20 embodiment, the dummy area of the second embodiment is disposed between the circuit area and the grid-line area. A manufacturing margin area is located on either side of the dummy area from the circuit area and grid-line area, respectively. Further,

as well as the first dummy patterns 202a in the first embodiment, the lower dummy pattern 300a of the second embodiment having the width (Lw) can be formed anywhere in the dummy area, preferably, the distance (L) between the edge 1000 of the chip area and an outer edge of the lower dummy pattern 300a is set for over 10 μm. Also, the circuit area is encompassed with the lower dummy pattern 300a.

5 Next, a borophosphosilicate glass (BPSG) layer 302 having a thickness of 800nm is formed on the silicon substrate and the lower dummy pattern 300a. The impurity concentrations of P2O5 and B2O3 in BPSG layer are 15wt% and 10wT%, respectively.

10 Then, a thermal treatment is performed to the BPSG layer 302 for thirty minutes at 900 C in the nitrogen atmosphere to planarize its surface. After that, an aluminum layer having a width of 600nm is formed on the BPSG layer 302, and then, metalized wiring patterns 304 are formed in the circuit area by etching the metal layer to make an interconnection of the circuit elements. Simultaneously, an upper dummy pattern 304a (first dummy pattern), which is electrically isolated from the wiring pattern 304, is

15 formed above the lower dummy pattern 300a. The shape and <sup>size</sup> side of the upper dummy pattern 304a are almost the same as the lower dummy pattern 302a.

Next, referring to Fig. 3B, a first insulating layer 306, such as silicon oxide layer, having a thickness of 200nm is formed by CVD on the surface of the BPSG layer 302, on the surface of metalized wiring patterns 304 and on the upper dummy pattern 304a.

20 Then, a SOG layer 308 as a second insulating layer is coated only on the first insulating layer 306 which the lower dummy pattern 300a is not formed thereunder to planarize the surface. That is, the SOG layer is not formed on the first insulating

layer 306 which is formed on the upper dummy pattern 304a. The condition not to be formed the SOG layer on the upper dummy pattern 304a is explained later. Then, a third insulating layer 310 having a thickness of 400nm is formed by CVD on the SOG layer 308 and on the exposed first insulating layer 306 which is formed on the upper dummy pattern 304a.

Then, referring to Fig.3C, the first insulating layer 306, the SOG layer 308, and the third insulating layer 310 on the grid line area are removed until the surface of the BPSG layer 302 is exposed.

In the process shown in Fig. 3B, the SOG layer 308 is coated in the following condition and the thickness of the SOG layer 308 on the upper dummy pattern 304a is measured in changing the width (Lw) of the lower and upper dummy pattern 302a, 304a or the length (Ls1) between the lower and upper dummy pattern 302a, 304a and metalized wiring pattern 304. A result of the measurement is shown in Fig. 4A.

- (4) the material of the SOG layer: Concentration of Solid content is 5.2wt%
- (5) the material of the SOG layer: Viscosity is 1.03 mPa.sec.
- (6) Rotary speed: 5000 rpm

Referring to Figs. 4A and 4B, the X axis shows the thickness of the SOG layer on the upper dummy pattern 304a, and Y axis shows the width (Lw) of the lower and upper dummy pattern 302a, 304a or length (Ls1) between the lower and upper dummy pattern 302a, 304a and metalized wiring pattern 304.

In Fig. 4A, the black circles shows the relationship between the thickness of the SOG layer and the width (Lw) of the lower and upper dummy pattern 302a, 304a

where the length ( $L_s$ ) is fixed to 2.6  $\mu\text{m}$  and the width ( $L_w$ ) is changed from 1 to 7  $\mu\text{m}$ .

In this case, it is found that the SOG layer becomes thicker if the width ( $L_w$ ) is designed for over  $2 \mu\text{m}$ . The with circles shows the relationship between the thickness of the SOG layer and the length ( $L_{s1}$ ) where the width ( $L_w$ ) is fixed to

5 1.0  $\mu\text{m}$  and the length ( $L_{s1}$ ) is changed from 0.9 to 5  $\mu\text{m}$ . In this case, it is found that  
the thickness of the SOG layer on the second dummy pattern 304a is maintained to  
nearly zero even if the length ( $L_{s1}$ ) is designed until 5  $\mu\text{m}$ .

As a result form this experimentation, if the width (Lw) is set to 1  $\mu\text{m}$  – 2  $\mu\text{m}$  the SOG layer is not formed on the upper dummy pattern 304a. Therefore, if the upper dummy pattern 304a having a width of 1  $\mu\text{m}$  – 2  $\mu\text{m}$  is formed, the SOG layer 308 which is adjacent to the grid-line area is completely isolated from the SOG layer 308 which is formed in the circuit area by the first insulating layer 306 formed on the upper dummy pattern 304a.

According to the second embodiment of the invention, in addition to the benefits  
15 of the first embodiment, the following advantages can be obtained.

Although the material of the lower dummy pattern 302a is not limited for the metal such as tungsten polycide, if it is formed of the conductivity material, metallized wiring patterns can be formed with the lower dummy pattern 302a. Further, the second embodiment of the invention can be adapted to any semiconductor device having multi-wiring layers without any additional processes. Furthermore, as the width (Lw) of the lower and upper dummy pattern 302a, 304a can be designed with a

range from 1  $\mu\text{m}$  to 2  $\mu\text{m}$ , it becomes easier to design the total semiconductor device.

The third embodiment is described below with reference to Figs. 5A through 5D. Referring to Fig. 5A, unillustrated circuit elements, such as transistors, are formed in a circuit area of the chip area on a main-surface of the semiconductor substrate 201, 5 and then, an unillustrated insulating layer is formed on the surface of the semiconductor substrate 201. Next, a metal layer which, is formed of Aluminum, is formed on the entire main-surface of the semiconductor substrate 201, and then, metalized wiring patterns 402 are formed in the circuit area by etching the metal layer to make an interconnection of the circuit elements. Simultaneously, a first dummy 10 pattern 402a, which is electrically isolated from the wiring pattern 402, is formed in a dummy area by etching the metal layer. As well as in the first and second embodiment, the dummy area is disposed between the circuit area and the grid-line area. A manufacturing margin area is located on either side of the dummy area from the circuit area and grid-line area, respectively. Further, as well as in the first 15 embodiment, the first dummy pattern 402a of the third embodiment having the width ( $L_w$ ) can be formed anywhere in the dummy area, preferably, the distance ( $L$ ) between the edge 1000 of the chip area and an outer edge of the first dummy pattern 402a is set for over 10  $\mu\text{m}$ . Also, the circuit area is encompassed with the first dummy pattern 402a.

20 Next, referring to Fig. 5B, a first insulating layer 404, such as silicon oxide layer, having a thickness of 200nm is formed by CVD on the entire surface of the semiconductor substrate 201. Then, a multi-SOG layer 406 as a second insulating

layer is formed on the first insulating layer 404 to planarize its surface. The multi-SOG layer 406 is formed by coating a SOG layer few times. That is, a first SOG layer is coated on the first insulating layer 404. Then, after it is dried up, a second SOG layer is coated on the dried SOG layer.

5 Next, referring to Fig. 5C, the multi-SOG layer is etched by the well-known RIE  
method under the conditions below until the surface of the first insulating layer 404 on  
the first dummy pattern 402a is exposed.

- (a) Gas flow rate: CHF<sub>3</sub>/CF<sub>4</sub>/Ar = 20/15/200 [sccm]
  - (b) Pressure: 40 [Pa]
  - (c) RF power: 200 [W]
  - (d) Etching rate of the multi-SOG layer: 7.5 [nm/sec]

Next, referring to Fig. 5D, the third insulating layer 408 having a thickness of 400nm is formed by CVD on the multi-SOG layer 406 and the exposed first insulating layer 404 which is formed on the first dummy pattern 402a..

15 Then, referring to Fig. 5E, the first insulating layer 404, the multi-SOG layer 406,  
and the third insulating layer 408 on the grid line area are removed until the surface of  
the semiconductor substrate 201 is exposed.

According to the third embodiment of the invention, in addition to the benefits of the first embodiment, the following advantages can be obtained. In the first and second embodiments, the SOG layer can not be formed thick. If it were formed thick, it would be formed on the first insulating layer on the first dummy pattern. However, as the multi-SOG layer can be formed thick in the third embodiment, the planarized

surface can be obtained in the circuit area.

The fourth embodiment is described below with reference to Fig. 7. Referring to Fig. 7, a pair of inner and outer dummy patterns 500a, 500b (a third dummy pattern and a first dummy pattern) are formed in the dummy area. Each dummy pattern has a same width ( $L_w$ ), and formed in the same method with the same size described in the first embodiment. The length ( $L_{s2}$ ) between the dummy patterns 500a, 500b is designed for over 0.9  $\mu\text{m}$ .

According to the fourth embodiment, in addition to the benefits of the first embodiment, the following advantages can be obtained.

Even If the SOG layer 504 is formed on the first insulating layer 502 on the outer dummy pattern 500b by accident, the semiconductor device can be protected from the moisture because the SOG layer 504 formed on the outer dummy pattern 500b is isolated from the SOG layer 504 formed in the circuit are by the insulating layer formed on the inner dummy pattern 500a.

The fifth embodiment is described below with reference to Figs. 7A and 7B. A bonding pad 601 is formed in a circuit area, and an outer dummy pattern 600a (a first dummy pattern) is formed in a dummy area. The size, location and manufacturing process of the outer dummy pattern is the same as the dummy pattern described in the first embodiment. That is, a width of the outer dummy pattern is designed for 1  $\mu\text{m}$ , and the length ( $L$ ) is designed for 10  $\mu\text{m}$ . A frame-shaped fourth dummy pattern 600b is formed for surrounding the bonding pad 601 in the circuit area. The distance ( $L_{s3}$ ) between the bonding pad 601 and the fourth dummy pattern 600b or

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the outer dummy pattern 600a is designed for over 0.9  $\mu\text{m}$ . The distance (Ls1) between the metalized wiring pattern 600 and the outer dummy pattern 600a or the fourth dummy pattern is designed for over 0.5  $\mu\text{m}$  because of the same reason described in the first embodiment. The metalized wiring pattern 600, the outer dummy pattern 600b and the fourth dummy pattern 600a are formed simultaneously by etching a conductive layer.

According to the fifth embodiment, in addition to the benefits of the first embodiment, the following advantages can be obtained. As the bonding pad 601 is surrounded by the fourth dummy pattern 600a, an SOG layer 606, which is exposed to an opening 602 for the bonding pad 601 is isolated to the SOG layer 606 which is formed in the circuit area. Therefore, it is possible to protect the semiconductor device from moisture which comes into the semiconductor device through the SOG layer 204 exposed to the opening 602.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. For example, although silicon oxide layers are used for the first and third insulating layer in the first through fifth embodiment, a silicon nitride layer, a PSG layer, a BPSG layer can be used. Further, it is possible to change the width of the dummy patterns in the first through fifth embodiment based on the concentration of solid content of the SOG layer. If a high concentrate material for the SOG layer is used, the dummy pattern having a wide width may be formed. On the contrary, if a low concentrate material for the SOG layer is used, the dummy pattern having a short width may be formed. Also,

in the third embodiment, it is possible to change the etching time based on the concentration of solid content of the SOG layer. Furthermore, in the second embodiment, the BPSG layer can be changed to other layer having thermal plagiarizing characteristics, such as a PSG layer. Various modifications of the illustrated embodiments, as well as other embodiments of the invention, will be apparent to those skilled in the art on reference to this description. Therefore, the appended claims are intended cover any such modifications or embodiments as fall within the true scope of the invention.

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